

CLAIMS

What is claimed is:

- 1 1. A method of downconverting a signal and rejecting an image, comprising:
 - 2 providing a first, second, third, fourth and fifth signal, wherein the first signal
 - 3 has a frequency F, the second signal has a frequency F/N, the third signal has a
 - 4 frequency F/N and is phase shifted 90° with respect the second signal; the fourth
 - 5 signal has a frequency F/NM, and the fifth signal has a frequency F/NM and is phase
 - 6 shifted 90° from the fourth signal;
 - 7 mixing the first signal with an input signal to produce a first mixer output
 - 8 signal;
 - 9 splitting the first mixer output signal to produce a first splitter output signal and
 - 10 a second splitter output signal;
 - 11 mixing the first splitter output signal with the second signal to produce a
 - 12 second mixer output signal;
 - 13 mixing the second splitter output signal with the third signal to produce a third
 - 14 mixer output signal;
 - 15 mixing the second mixer output signal with the fourth signal to produce a
 - 16 fourth mixer output signal;
 - 17 mixing the third mixer output signal with the fifth signal to produce a fifth mixer
 - 18 output signal; and
 - 19 combining the fourth mixer output signal and the fifth mixer output signal to
 - 20 produce a combiner output signal.

1 2. The method of Claim 1, wherein mixing the first splitter output signal with the
2 second signal to produce a second mixer output signal further comprises low-pass
3 filtering.

1 3. The method of Claim 2, wherein mixing the second splitter output signal with
2 the third signal to produce a third mixer output signal further comprises low-pass
3 filtering.

1 4. The method of Claim 1, wherein N and M are integers greater than 1.

1 5. The method of Claim 4, wherein N and M are each multiples of 2.

1 6. The method of Claim 3, wherein providing the second, third, fourth, and fifth
2 signals comprises digitally dividing the first signal.

1 7. The method of Claim 5, wherein N equals 2 and M equals 4.

1 8. The method of Claim 3, wherein F is a frequency in the range of 3.113 GHz to
2 3.545 GHz.

1 9. The method of Claim 8, wherein the input signal has a frequency in the range
2 of 5.15 GHz to 5.825 GHz.

1 10. The method of Claim 9, wherein the combiner output signal has a frequency
2 of 90 MHz.

1 11. A method of upconverting a signal, and rejecting an image, comprising:

2 providing a first, second, third, fourth and fifth signal, wherein the first signal
3 has a frequency F, the second signal has a frequency F/N, the third signal has a
4 frequency F/N and is phase shifted 90° with respect the second signal; the fourth
5 signal has a frequency F/NM, and the fifth signal has a frequency F/NM and is phase
6 shifted 90° from the fourth signal;

7 splitting an input signal to produce a first splitter output signal a and second
8 splitter output signal;

9 mixing the first splitter output signal with the fifth signal to produce a first
10 mixer output signal;

11 mixing the second splitter output signal with the fourth signal to produce a
12 second mixer output signal;

13 high-pass filtering the first mixer output signal and the second mixer output
14 signal to produce, respectively a first filter output and a second filter output;

15 mixing the first filter output with the third signal to produce a third mixer output
16 signal;

17 mixing the second filter output with the second signal to produce a fourth
18 mixer output signal;

19 combining the third mixer output signal and the fourth mixer output signal to
20 produce combiner output signal; and

21 mixing the combiner output signal with the first signal to produce a transmitter
22 output signal.

1 12. The method of Claim 11, wherein N and M are integers greater than 1.

1 13. The method of Claim 12, wherein N and M are each multiples of 2.

1 14. The method of Claim 11, wherein providing the second, third, fourth, and fifth
2 signals comprises digitally dividing the first signal.

1 15. The method of Claim 13, wherein N and M each equal 4.

1 16. A method of rejecting an image, comprising:

2 mixing an input signal with a local oscillator signal to produce a first
3 intermediate frequency signal;

4 splitting the first intermediate frequency signal into a first part and a second
5 part;

6 mixing the first part with a first clock signal to produce a first second-
7 intermediate-frequency signal, and mixing the second part with a second clock
8 signal, to produce a second second-intermediate-frequency signal;

9 filtering the first and second second-intermediate-frequency signals;

10 mixing the filtered first second-intermediate-frequency signal with a third clock
11 signal to produce a first third-intermediate-frequency signal, and mixing the filtered
12 second second-intermediate-frequency signal with a fourth clock signal to produce a
13 second third-intermediate-frequency signal; and

14 combining the first third-intermediate-frequency signal with the second third-
15 intermediate-frequency signal to produce an output signal;

16 wherein the first and second clock signals have a frequency that is less than
17 that of the local oscillator by a factor of N, and the second clock signal is phase

18 shifted 90° from the first clock signal, the third and fourth clock signals have a
19 frequency that is less than that of the local oscillator by a factor of NM, and the
20 fourth clock signal is phase shifted 90° from the third clock signal, and N and M are
21 integers greater than one.

1 17. The method of Claim 16, wherein N is a multiple of 2.

1 18. The method of Claim 16, wherein M is a multiple of 2.

1 19. The method of Claim 16, wherein N and M are each a multiple of 2.

1 20. The method of Claim 16, wherein the image is rejected in a receiver.

1 21. The method of Claim 16, wherein the image is rejected in a receiver, N and M
2 are each a multiple of 2, and the filtering comprises low-pass filtering.

1 22. A method of rejecting an image, comprising:
2 splitting a transmit baseband signal into a first part and a second part;
3 mixing the first part with a first clock signal to produce a first second-
4 intermediate-frequency signal, and mixing the second part with a second clock
5 signal, to produce a second second-intermediate-frequency signal;
6 high-pass filtering the first second-intermediate-frequency signal, and high-
7 pass filtering the second second-intermediate-frequency signal;

8 mixing the high-pass filtered first second-intermediate-frequency signal with a
9 third clock signal to produce a first third-intermediate-frequency signal, and mixing
10 the high-pass filtered second second-intermediate-frequency signal with a fourth
11 clock signal to produce a second third-intermediate-frequency signal;
12 combining the first third-intermediate-frequency signal with the second third-
13 intermediate-frequency signal to produce a combined signal; and
14 mixing the combined signal with a local oscillator signal to produce a transmit
15 output signal;
16 wherein the first and second clock signals have a frequency that is less than
17 that of the local oscillator by a factor of NM, and the second clock signal is phase
18 shifted 90° from the first clock signal, the third and fourth clock signals have a
19 frequency that is less than that of the local oscillator by a factor of N, and the fourth
20 clock signal is phase shifted 90° from the third clock signal, and N and M are
21 integers greater than one.

1 23. The method of Claim 22, wherein N and M are multiples of 2.

1 24. The method of claim 23, wherein the second part of the split transmit
2 baseband signal is phase-shifted 180 degrees from the first part of the split transmit
3 baseband signal.

1 25. An image rejection circuit, comprising:
2 a local oscillator, a first divider coupled to the local oscillator, and a second
3 divider coupled to the first divider network;

4 a first mixer having a first and second input terminals, and an output terminal;

5 a first splitter having an input terminal coupled to the output terminal of the

6 first mixer, and having a first and a second splitter output terminal;

7 a second mixer having a first input terminal coupled to the first output terminal

8 of the first splitter, a second input terminal coupled to an in-phase output terminal of

9 the first divider, and having an output terminal;

10 a third mixer having a first input terminal coupled to the second output

11 terminal of the first splitter, a second input terminal coupled to a quadrature-phase

12 output terminal of the first divider, and having an output terminal;

13 a first filter coupled to the second mixer output terminal, and a second filter

14 coupled to the third mixer output terminal;

15 a fourth mixer having a first input terminal coupled to the first filter, a second

16 input terminal coupled to an in-phase output terminal of the second divider, and

17 having an output terminal;

18 a fifth mixer having a first input terminal coupled to the second filter, a second

19 input terminal coupled to a quadrature-phase output terminal of the second divider,

20 and having an output terminal; and

21 a combiner having a first input terminal coupled to the output terminal of the

22 fourth mixer, a second input terminal coupled to the output terminal of the fifth mixer,

23 and having an output terminal.

1 26. The circuit of Claim 25, wherein the in-phase and quadrature-phase output

2 terminals of the first divider are adapted to provide signals that are phase shifted 90°

3 from each other.

1 27. The circuit of Claim 26, wherein the in-phase and quadrature-phase output
2 terminals of the first divider are adapted to provide signals that are the same
3 frequency as each other, and that frequency is less than that of the local oscillator by
4 a first factor which is a multiple of 2.

1 28. The circuit of Claim 27, wherein the in-phase and quadrature-phase output
2 terminals of the second divider are adapted to provide signals that are the same
3 frequency as each other, and that frequency is less than that of the local oscillator by
4 a second factor which is a multiple of 2.

1 29. The circuit of Claim 28, wherein the second factor is greater than the first
2 factor.

1 30. The circuit of Claim 25, wherein the first filter and the second filter are each
2 low-pass filters.

1 31. The circuit of Claim 25, wherein the first input terminal of the first mixer is
2 coupled to an input signal source.

1 32. The circuit of Claim 31, wherein the second input terminal of the first mixer is
2 coupled to the local oscillator.

1 33. An image rejection circuit, comprising:
2 a local oscillator, a first divider coupled to the local oscillator, and a second
3 divider coupled to the first divider;

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4 a first splitter having an input terminal coupled to an input signal source, a first
5 output terminal and a second output terminal;
6 a first mixer having a first input terminal coupled to the first output terminal of
7 the first splitter, a second input terminal coupled to a second output terminal of the
8 second divider, and an output terminal;
9 a first high-pass filter coupled to the output terminal of the first mixer;
10 a second mixer having a first input terminal coupled to the second output
11 terminal of the first splitter, a second input terminal coupled to a first output terminal
12 of the second divider, and an output terminal;
13 a second high-pass filter coupled to the output terminal of the second mixer;
14 a third mixer having a first input terminal coupled to first high-pass filter, a
15 second input terminal coupled to a second output terminal of the first divider, and an
16 output terminal;
17 a fourth mixer having a first input terminal coupled to the second filter, a
18 second input terminal coupled to a first output terminal of the first divider, and having
19 an output terminal;
20 a combiner having a first input terminal coupled to the output terminal of the
21 third mixer, a second input terminal coupled to the output terminal of the fourth
22 mixer, and an output terminal; and
23 a fifth mixer having a first input terminal coupled to the output terminal of the
24 combiner, a second input terminal coupled to an output of the local oscillator, and
25 having an output terminal.

1 34. The circuit of Claim 33, wherein the input terminal of the first splitter is
2 coupled to an input signal source.

1 35. The circuit of Claim 33, wherein the input terminal of the first splitter is
2 coupled to a transmit baseband signal source.

1 36. The circuit of Claim 33, wherein the first divider and the second divider each
2 divide by factor wherein the factor is a multiple of 2.

1 37. An image rejection circuit, comprising:
2 a local oscillator, a first divider coupled to the local oscillator, and a second
3 divider coupled to the local oscillator;
4 a first mixer having two input terminals and an output terminal;
5 a first splitter having an input terminal coupled to the output terminal of the
6 first mixer, and having a first and a second splitter output terminal;
7 a second mixer having a first input terminal coupled to the first output terminal
8 of the first splitter, a second input terminal coupled to an in-phase output terminal of
9 the first divider, and having an output terminal;
10 a third mixer having a first input terminal coupled to the second output
11 terminal of the first splitter, a second input terminal coupled to a quadrature-phase
12 output terminal of first divider, and having an output terminal;
13 a first filter coupled to the second mixer output terminal, and a second filter
14 coupled to the third mixer output terminal;
15 a fourth mixer having a first input terminal coupled to the first filter, a second
16 input terminal coupled to an in-phase output terminal of the second divider, and
17 having an output terminal;
18 a fifth mixer having a first input terminal coupled to the second filter, a second
19 input terminal coupled to a quadrature-phase output terminal of the second divider,
20 and having an output terminal; and

21 a combiner having a first input terminal coupled to the output terminal of the
22 fourth mixer, a second input terminal coupled to the output terminal of the fifth mixer,
23 and having an output terminal.

1 38. The circuit of Claim 37, wherein the first divider and the second divider each
2 divide by factor wherein the factor is a multiple of 2.

1 39. An image rejection circuit, comprising:
2 a local oscillator, a first divider coupled to the local oscillator, and a second
3 divider coupled to the local oscillator;
4 a first splitter having an input terminal coupled to an input signal source, a first
5 output terminal and a second output terminal;
6 a first mixer having a first input terminal coupled to the first output terminal of
7 the first splitter, a second input terminal coupled to a second output terminal of the
8 second divider, and an output terminal;
9 a first high-pass filter coupled to the output terminal of the first mixer;
10 a second mixer having a first input terminal coupled to the second output
11 terminal of the first splitter, a second input terminal coupled to a first output terminal
12 of the second divider, and an output terminal;
13 a second high-pass filter coupled to the output terminal of the second mixer;
14 a third mixer having a first input terminal coupled to first high-pass filter, a
15 second input terminal coupled to a second output terminal of the first divider, and an
16 output terminal;
17 a fourth mixer having a first input terminal coupled to the second filter, a
18 second input terminal coupled to a first output terminal of the first divider, and having
19 an output terminal;

20 a combiner having a first input terminal coupled to the output terminal of the
21 third mixer, a second input terminal coupled to the output terminal of the fourth
22 mixer, and an output terminal; and

23 a fifth mixer having a first input terminal coupled to the output terminal of the
24 combiner, a second input terminal coupled to an output of the local oscillator, and
25 having an output terminal.

1 40. The circuit of Claim 39, wherein the first divider and the second divider each
2 divide by factor wherein the factor is a multiple of 2.

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